REMARKS

Claims 1-6 were previously pending in the application.

The specification has been amended to correct typographical or editorial errors.

Claims 1-6 are amended. In particular, claim 1 is amended to add a limitation reciting forming an etch stop layer. Support for this amendment is in the Specification on page 8, lines 28-29.

New claims 7-9 are added. Support for new claim 7 is in the Specification on page 9, lines 18-35.

No new matter is added.

Claims 1-9 remain in the case.

Applicant requests reconsideration and allowance of the claims in the light of the above amendment and following remarks.

Claim Rejections - 35 USC § 102

Claims 1-4 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,869,396, Pan et al., ("Pan").

Applicant respectfully traverses the rejections.

Claim 1 is currently amended to recite,

"*forming an etch stop layer overlying the resulting structure including the gate lines*;

forming an interlayer insulating layer *on said etch stop layer*;

exposing a surface of said silicon gate layer of said gate lines through said etch stop layer." See, for example, the etch stop layer 139 (applicant's Fig. 7) overlying the gate structures 133.

Pan does not, however, teach or disclose the above-limitations of amended claim 1. Figs. 1-5 of Pan clearly show gate structures (14a plus 16a), with no overlying etch stop layer. In Figure 1 of Pan, a pre-metal dielectric layer 22 is formed on the gate structures 16a without "*forming an etch stop layer overlying the resulting structure including the gate lines*," as recited in claim 1. Therefore, for at least this reason, amended claim 1 is not anticipated by Pan, and removal of the rejection is requested.

Claim 2 recites exposing said silicon gate layer of said gate lines includes planarizing said silicon layer. In other words, for example, referring to Figs. 8A and 9A of the present application, the silicon layer 140 is planarized with the interlayer insulation layer 141. Subsequently, a metal silicide layer is formed on the planarized silicon layer 145 (Figure 9A).

In contrast, Pan does not teach or disclose "exposing said silicon gate layer of said gate lines includes planarizing said silicon layer," as recited in claim 2. In other words, it is impossible for Pan to teach or disclose the above limitations, because Pan has not yet created the silicon layer (contacting stud 28a, figure 4) until after Pan adds patterned pre-metal dielectric layers 26 (col. 10, lines 17-20). For at least this reason, claim 2 is not anticipated by Pan, and removal of the rejection is requested. Also, Pan does not anticipate the limitation of new claim 7, which recites, "forming a silicide layer on said planarized silicon layer."

The applicant asserts that claim 3, which recites additional novel and non-obvious features of its base claim, is also in condition for allowance for its dependency and its own merits.

Claims 4-6 Rejection

Claims 4-6 can be rejected under 35 U.S.C. § 102(e), or possible a 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,376,876 B1, Shin, et al., ("Shin"), or Shin with a secondary reference.

Applicant respectfully traverses the rejections.

None of the cited references teach or disclose all of the limitations of claim 4, for example, "forming a metal silicide layer on exposed upper surfaces of said gate lines and on said silicon common source line." Thus, claim 4 is allowable.

Further, none of the cited references teach or disclose, "forming an etch stop layer over said substrate between said doping and said forming said lower interlayer insulating layer," as recited in claim 5. Thus, claim 5 is allowable.

The applicant also asserts that claim 6, which recites additional novel and non-obvious features of its base claim, is also in condition for allowance for its dependency and its own merits.

In the alternative, as suggested by the Examiner, applicant respectfully submits that the present application and the Shin patent are subject to common ownership in Samsung Electronics Co. Ltd., at the time the invention was made, and thus claims 4-6 are allowable.

In Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-9 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Hosoon Lee
Limited Recognition Under 37 CFR § 10.9(b)

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613

I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (703) 872-9306, on December 20, 2004.

Stormi R. Davis